

IN THE SPECIFICATION:

Please replace paragraph number [0002] with the following rewritten paragraph:

[0002] State of the Art: Semiconductor devices, from microprocessors to memory chips, are fabricated by performing a long series of processes including depositing various materials, selectively ~~masking~~ masking, and etching on a semiconductor wafer or other bulk semiconductor substrate. Many identical integrated circuits may be fabricated on a single semiconductor wafer by forming ~~them~~ the integrated circuits in arrays of semiconductor die locations across the wafer. Ultimately, semiconductor dice bearing the individual integrated circuits are singulated from the wafer and are either further processed, including packaging and additional testing, or discarded when they are determined to be defective in one or more aspects and the defect or defects cannot be remediated.

Please replace paragraph number [0006] with the following rewritten paragraph:

[0006] A considerable advantage in cost ~~and in~~ and process time could be attained by burning-in and testing a semiconductor wafer before it is singulated into discrete devices. Additional savings may be recognized by forgoing packaging of devices that ultimately fail once subjected to burn-in conditions. A considerable effort has been expended to develop effective methods for wafer level testing. One such approach utilizes cantilevered or spring-wire probes which are placed on a contactor or probe card for simultaneous contact to all of the devices on the semiconductor wafer. Such contactor cards are expensive to manufacture and result in undesirable electrical characteristics such as increased inductance along parallel wires. Furthermore, conventional contactor cards are generally fabricated from materials having dissimilar expansion coefficients than the semiconductor substrate, for example, a semiconductor wafer (hereinafter "wafer-under-test") undergoing testing. Therefore, conventional contactor cards exhibit a markedly dissimilar expansion to the wafer-under-test over temperature extremes characteristic of burn-in testing and may result in misalignment of the contactor card contact pins

with the corresponding integrated circuit contact pads (bond pads) on the semiconductor wafer-under-test.

Please replace paragraph number [0008] with the following rewritten paragraph:

[0008] The present invention comprises, in various embodiments, a compliant contact structure, a contactor card and test system including ~~same same~~, and methods of fabrication and use associated therewith. In one embodiment of the present invention, a compliant contact structure includes a substantially planar substrate having a thickness, including a compliant contact being secured therein and extending transversely thereto. The compliant contact includes a portion fixed within the substrate and at least another portion integral with the fixed portion and laterally unsupported within the thickness of the substrate and extending therebeyond. Opposing portions of the same compliant contact may be unsupported to provide a dual-sided compliant contact structure, with a medial portion of the contact fixed to the substrate. Adjacent compliant contact structures having laterally unsupported portions extending beyond opposing sides of the substrate may be mutually operably coupled to provide a dual-sided compliant contact ~~structure~~ structure.

Please replace paragraph number [0009] with the following rewritten paragraph:

[0009] In another embodiment of the present invention, a method for forming a compliant contact structure is provided. A contact slot extending between a first side and a second side of a substantially planar substrate is formed at a selected location. The contact slot is filled with a conductive material to form a conductive pin. A portion of the substrate immediately surrounding and laterally supporting a portion of the conductive pin is removed to a selected depth within the substrate with the remaining portion of the conductive pin remaining fixed to the substrate, the thickness of the substrate also being generally reduced adjacent the removed portion of the substrate. The exposed, unsupported portion of the conductive pin extends beyond the substrate and provides a compliant contact element. Opposing portions of the substrate may be removed to leave a medial portion of the conductive pin supported and thus

form a dual-sided compliant contact structure. ~~Adjacent-Adjacent~~, but opposingly ~~facing~~ facing, compliant contacts may be formed and operably coupled to form a dual-sided compliant contact structure.

Please replace paragraph number [0014] with the following rewritten paragraph:

[0014] FIGS. ~~2A—2F~~ 2A–2F are cross-sectional views illustrating a sequence of processing steps for fabricating a compliant contact structure according to an embodiment of the present invention;

Please replace paragraph number [0021] with the following rewritten paragraph:

[0021] The present invention, according to the various embodiments described herein, is drawn to compliant contact structures, methods of fabricating ~~same~~ same, and methods for testing using the compliant contact structures. The various views and diagrams are illustrated generally as cross sectional views for clarity; however, the specific formed profiles and devices may be arranged across the surface of the substrate and with various orientations and geometries appreciated by those of ordinary skill in the art.

Please replace paragraph number [0022] with the following rewritten paragraph:

[0022] While, the various embodiments of the present invention find general application to providing electrical coupling in small dimensions, one exemplary specific application of the various embodiments includes the formation of one or more compliant contact structures for use in conjunction with the fabrication of a contactor card for coupling to integrated circuits on a semiconductor substrate such as, for example, a semiconductor wafer-under-test during wafer level test probing of semiconductor wafers. By way of example, FIG. 1 illustrates a generally planar substrate 10 having defined thereon one or more locations 12 for the formation of a compliant contact structure. In an exemplary embodiment of the present invention, substrate 10 exhibits ~~an~~ a coefficient of thermal expansion (CTE) similar to the CTE of a semiconductor substrate bearing integrated circuitry to be tested in order to minimize any potential for

temperature-induced contact misalignment over temperature extremes. For example and not by way of limitation, substrate 10 may itself comprise a semiconductor material such as silicon, or a ceramic exhibiting a CTE similar to that of silicon.

Please replace paragraph number [0024] with the following rewritten paragraph:

[0024] By way of further example and not limitation, contact slot 14 may also be formed through chemical etching or mechanical machining techniques. While chemical etching and mechanical drilling or boring are contemplated as within the scope of the present invention, laser machining generally provides improved processing time over each of the other techniques. Using the exemplary laser at a pulse rate of 40 kHz, approximately 3-5 microns of substrate depth may be ablated with the activation of each ~~pulse~~ pulse, which is a marked improvement over etch rates achievable by chemical etching processes (e.g., a dry etch process), is more controllable than a wet ~~etch~~ etch, and is less likely to cause unacceptable collateral damage to substrate 10 than mechanical machining.

Please replace paragraph number [0025] with the following rewritten paragraph:

[0025] ~~Further~~ Further, by way of example and not limitation, the relative lateral dimensions of contact slot 14 are sized so as to provide a compliant coupling mechanism with a prospective mating substrate such as, for example, a semiconductor wafer-under-test having integrated circuits thereon. While FIGS. 1 and 1A illustrate contact slot 14 as being rectangular in nature, other geometries are also contemplated including square, circular, oval or elliptical and other polygonal profiles. Slot configuration in the X-Y plane, the plane of the substrate 10, may be selected to provide a preferential direction for bending of the compliant contact. The dimensions of contact slot 14 may be determined by several factors including the ~~resiliency~~ resiliency of the selected conductive composition or metal for filling contact slot 14 and the mating interface dimensions, for example, of the contact pad of the semiconductor device to be tested, such as a wafer-under-test. By way of example only, the dimensions of contact slot 14 may assume dimensions on the order of 10-20 microns by 60-80 microns.

Please replace paragraph number [0026] with the following rewritten paragraph:

[0026] As a further process in the formation of contact slot 14, when laser machining or other coarse substrate removal techniques are utilized, a cleaning process may further be employed to soften any rough edges and to clean any heat-damaged substrate (commonly termed the “heat affected ~~zone~~”, zone,” or HAZ) from the respective contact slots 14. By way of example and not limitation, if substrate 10 is formed of silicon, an exemplary cleaning process may include TetraMethyl Ammonium Hydroxide (TMAH) or Propylene Glycol TMAH as an etching agent. Other substrate post-process cleaning processes are contemplated and the specific application of these processes is known by those of ordinary skill in the art and is not further ~~describe~~ described herein.

Please replace paragraph number [0028] with the following rewritten paragraph:

[0028] Regarding FIG. 2B, substrate 10, in one embodiment of the present invention, is comprised of a semiconductive material such as silicon which, if directly coupled to a target contact pad of a semiconductor substrate such as a wafer-under-test having integrated circuits thereon, may present undesirable loading or shorting to the electronic circuitry under test. If substrate 10 is comprised of a semiconductive or conductive material, then electrical conductivity of the compliant contact structure to be formed on substrate 10 is passivated by forming an insulative or dielectric layer 20 on sidewalls 18 of contact slot 14 which coats contact slot 14 by coating the substrate 10 with a suitable dielectric material appropriate for the type of composition of substrate 10. The dielectric layer 20 may be comprised of spin-on-glass, thermal oxide, Parylene™ polymer, silicon dioxide, silicon nitride, silicon oxynitride, a glass, *i.e.*, borophosphosilicate glass, phosphosilicate glass or borosilicate glass, or any dielectric having a low dielectric constant known by those of ordinary skill in the art. To accomplish the passivation, the dielectric layer 20 may be deposited or formed to any desired thickness using any known process suitable for the dielectric material in question including, without limitation, physical vapor deposition (PVD), ~~CVD~~ chemical vapor deposition (CVD), low pressure chemical vapor deposition (LPCVD), rapid thermal nitridation (RTN), a spin-on-glass (SOG) process,

flow coating or any other known process. In other embodiments, the dielectric layer 20 may comprise an insulating polymer, such as BT resin, polyimide, benzocyclobutene or polybenzoxazole deposited using an injection or capillary process or a vacuum draw. The insulative layer 20 may be, for example, of about 1 to 5 μm in thickness. If substrate 10 comprises an electrically insulating material, such as suitable ceramic, then dielectric layer 20 may be omitted.

Please replace paragraph number [0029] with the following rewritten paragraph:

[0029] A seed layer may be used to form a catalyst for the deposition of an electrically conductive layer within contact slot 14. As shown in FIG. 2B, a seed layer 22 of a conductive material may be deposited over the outer surface 24 and inner surface 26 of the contact slot 14 and coats the insulative layer 20. In the illustrated embodiment, the seed layer 22 comprises titanium nitride (TiN) and is deposited by CVD. Other materials that may be used as the seed layer 22 include, without limitation, titanium (Ti), silicon nitride (Si_3N_4), a polysilicon, palladium-~~(Pd)~~ (Pd), and tin (Sn). Other deposition processes that may be used to deposit a seed layer 22 include PVD, vacuum-~~evaporation~~ evaporation, and sputtering. It will be apparent that the selection of the type of material and deposition process utilized to deposit the seed layer 22 may vary depending on the type of desired material used to form the electrically conductive portion of the compliant contact structure within the contact slot 14.

Please replace paragraph number [0034] with the following rewritten paragraph:

[0034] FIG. 2E illustrates a further processing step for forming a compliant contact structure, in accordance with an embodiment of the present invention. As shown, a contact bulk pit 32 is formed on a contact or first side of substrate 10 beginning at a contact side original surface 34 and extending into the thickness T of substrate 10 while circumscribing conductor 30. While various substrate removal techniques are contemplated, including chemical and mechanical etching, laser 16 illustrates use of an ablation process for forming the contact bulk pit 32 within substrate 10. Because of the collateral effects of laser ablating and further due to

the relatively imprecise nature of laser machining, contact sidewalls 36 of substrate material are retained around conductor 30. The dimensions of the contact bulk pit 32 are determinable based upon the lateral cross-sectional (X-Y plane) dimensions of conductor 30 which will, in part and in combination with the conductive material selected for ~~conductor~~ conductor 30, determine the stiffness or resiliency of the compliant contact structure being formed. By way of example, for a substrate of approximately 750 microns thickness, an exemplary depth of the contact bulk pit 32 may be approximately 300 microns while the width of one side of the contact bulk pit 32 may be approximately 100 microns. The depth of the contact bulk pit 32 generally defines the approximate length of the flexible portion of the resulting ~~compliant~~ compliant contact structure.

Please replace paragraph number [0036] with the following rewritten paragraph:

[0036] Additionally, the substrate material removal process used for removal of contact sidewalls 36 also provides exposure of laterally unsupported portion 40 of compliant contact structure 54 beyond substrate 10 by recessing the original surface 34 of substrate 10 by a compliance distance 44 to form a contact side stop 46. The recessing of contact side stop 46 from the original location of original surface 34 induces flexure of laterally unsupported portion 40 of compliant contact structure 54 during coupling of compliant contact structure 38 with a semiconductor substrate bearing integrated circuitry to be tested. FIG. 3 illustrates the coupling of compliant contact structure-~~38~~ 54 with a contact pad 50 of an exemplary semiconductor substrate comprising a wafer-under-test 52. As noted above, removal of contact sidewalls 36 (FIG. 2E) further results in the formation of a contact recess 42 (FIG. 2F) configured to accept therein without interference a contact pad 50 of, for example, the wafer-under-test 52 operably coupled to portion 40 of compliant contact structure 54. Electrical continuity from compliant contact structure 54 may be extended to another location on substrate 10 opposite the surface disposed adjacent the wafer-under-test 52 by forming a rerouting conductor element 56 contiguous with portion 48 of conductor 30 of compliant contact structure 54 fixed within substrate 10 and extending thereover. Rerouting conductor element 56

may be employed to place contacts on substrate 10 for coupling with a probe assembly operably coupled to a tester.

Please replace paragraph number [0038] with the following rewritten paragraph:

[0038] For the dual-sided compliant contact structure of FIGS. 4A-4B, the preliminary processing steps are not illustrated; however, processing proceeds according to the sequence described with respect to FIGS. 2A-2D wherein a substrate 110 has formed therein a contact slot through the entire thickness dimension of the substrate 110. When necessary, the substrate within the contact slot is passivated by an insulative layer 120 and a conductor 130 is formed within the contact slot. Specifically illustrated in FIG. 4A are further processing steps, namely the formation of a first contact bulk pit 132 formed on a first side 126 of substrate 110 beginning at a first original surface 134 and further circumscribing conductor 130 on the first side 126. Furthermore, a second contact bulk pit 136 is formed on a second side 128 of substrate 110 beginning at a second original surface 138 and further circumscribing conductor 130 on the ~~second-side~~ original surface 138. The substrate material in the contact bulk pits 132, 136 may be removed according to one or more of the substrate removal techniques previously described. When laser machining is selected, contact sidewalls 140 and 142 are initially retained around conductor 130. The dimensions of the contact bulk pits 132, 136 are determinable based upon the aforementioned criteria and are not further described herein.

Please replace paragraph number [0039] with the following rewritten paragraph:

[0039] FIG. 4B illustrates a further substrate removal process for forming a dual-sided compliant contact structure 144. A further substrate removal process includes one of the substrate etching processes described above which is preferential for the material of substrate 110, for example silicon, and preferentially does not etch the conductor 130. One example of such a preferential etch process is a TMAH: glycol wet etch process. The selected etch process removes portions of substrate 110 including contact sidewalls 140, 142 (FIG. 4A) and ~~dielectric~~ insulative layer 120 resulting in a dual-sided compliant contact 146 which includes

on a first side thereof laterally unsupported portion 148 of conductor 130, a second side laterally unsupported portion 150 and a common portion 152 of conductor 130 fixed within substrate 110. ~~Portion~~Common portion 152 may be retained securely within substrate 110 in electrical isolation therefrom due to the presence of ~~dielectric~~ insulative layer 120 (where required) to facilitate electrical continuity and structural support of laterally unsupported portions 148, 150 of conductor 130.

Please replace paragraph number [0040] with the following rewritten paragraph:

[0040] Additionally, the substrate material removal process also creates exposure of ~~dual~~-dual-sided compliant contact 146 by respectively recessing the first original surface 134 and second original surface 138 of substrate 110 by first and second compliance distances 154, 156 to form first and second contact side stops 158, 160. As previously stated with respect to the prior embodiment, the recessing of contact side stops 158, 160 induces flexure of laterally unsupported portions 148, 150 of compliant contact 146 during coupling of dual-sided compliant contact structure 144 with corresponding interfaces. While the dual-sided compliant contact structure 144 is illustrated as comprising symmetric first and second side compliant contact elements 162, 164, asymmetric contact structures on first and second sides of a substrate are also contemplated. For example, exposure ~~and thus~~ and flexure of compliant contact elements 162, 164 may differ.

Please replace paragraph number [0041] with the following rewritten paragraph:

[0041] FIG. 5 illustrates the coupling of a dual-sided compliant contact structure 144 embodied in a dual-sided contactor card 166 with a contact pad 50 of a semiconductor substrate such as a wafer-under-test 52 and a contact pad 51 of a test probe card 53. Coupling of wafer-under-test 52 with test probe card 53 results in the corresponding compliant response in respective first and second side laterally unsupported portions 148, 150 comprising compliant contact elements 162, 164 of dual-sided compliant contact 146. As is evident in FIG. 5, side stops 158, ~~150~~ 160 limit the maximum flexure travel of compliant contact elements 162, 164

when another substrate such as a wafer-under-test or a test probe card is placed adjacent substrate 110.

Please replace paragraph number [0042] with the following rewritten paragraph:

[0042] FIGS. 6A-6B illustrates a dual-sided complex compliant contact structure comprising operably coupled compliant contact structures similar to those described in conjunction with FIGS. 2A-2F and 3 in accordance with another embodiment of the present invention. This embodiment facilitates the formation of compliant contacts projecting from both sides of a substrate to accommodate formation of an offset contactor card arrangement. For the dual-sided compliant contact structure of FIGS. 6A-6B, the preliminary processing steps are not illustrated; however, processing proceeds according to the sequence described with respect to FIGS. 2A-2D wherein a substrate 210 has formed therein three contact slots ~~at locations~~ 172, 174, ~~176~~ 176 through the entire thickness dimension of the substrate 210. When necessary due to the material selected for substrate 210, the substrate material within the contact slots 172, 174, 176 is electrically isolated by dielectric layers (not shown herein for clarity) and individual conductors 178-182 are formed within the respective contact slots ~~at locations~~ 172, 174, 176. The linking conductor 180 may be fabricated to provide an electrical interconnection between conductors 182 and 178. Specifically illustrated in FIG. 6A are further processing steps, namely the formation of a first contact bulk pit 232 is formed on a first side 226 of substrate 210 beginning at a first original surface 234 and further circumscribing conductor 182 on the first side 226. Furthermore, a second contact bulk pit 236 is formed on a second side 228 of substrate 210 beginning at a second original surface 238 and further circumscribing conductor 178 on the second side 228. The substrate material in the contact bulk pits 232, 236 may be removed according to one or more of the substrate removal techniques previously described. When laser machining is selected, contact sidewalls 240 and 242 are initially retained around conductors 182, 178, respectively.

Please replace paragraph number [0043] with the following rewritten paragraph:

[0043] FIG. 6B illustrates a further substrate removal process for further forming a dual-sided compliant contact structure 244. A further substrate removal process includes one of the substrate etching processes described above which is preferential for the material of substrate 210, for example silicon, and preferentially does not etch the conductors 178, 180, 182. One example of such a preferential etch process is a TMAH wet etch process. The selected etch process removes portions of substrate 210 including contact sidewalls 240, 242 (FIG. 6A) resulting in a dual-sided compliant contact 246 which includes on a first ~~side~~ side, laterally unsupported portion 248 secured in substrate 210 by portion 252 of conductor 182 ~~and~~ and, on a second ~~side~~ side, laterally unsupported portion 250 secured in substrate 210 by portion 253 of conductor 178. As shown in FIG. 6B, additional electrically conductive traces 272, 274 may be formed on the opposing sides of substrate 210 to electrically couple together conductors 178 and 182 via linking conductor 180. Similar to the previous embodiments, the substrate material removal process also creates additional exposure for laterally unsupported portions 248, ~~252~~ 250 by recessing the first original surface 234 and second original surface 238 of substrate 210 by first and second compliance distances 254, 256 to form first and second contact side stops 258, 260. The ends of linking conductor 180 will also be exposed by the etching process, and may be selectively removed as by abrasion prior to formation of electrically conductive traces 272, 274. As previously stated, the recessing of contact side stops 258, 260 induces flexure of laterally unsupported portions 248, 250 during coupling of dual-sided compliant contact structure 244 with other substrates placed adjacent to substrate 210. Furthermore, while the dual-sided ~~complex compliant~~ contact structure 244 is illustrated as comprising linked, symmetric first and second side contact ~~structure~~ structures 262, 264, asymmetric contact structures on first and second sides are also contemplated. For example, exposure and thus flexure of laterally unsupported portions 248, ~~252~~ 250 may differ.

Please replace paragraph number [0044] with the following rewritten paragraph:

[0044] FIG. 7 illustrates the coupling of a dual-sided compliant contact structure 244 embodied in a dual-sided contactor card 266 with a contact pad 50 of a semiconductor substrate such as a wafer-under-test 52 and a contact pad 51 of a test probe card 53. Coupling of wafer-under-test 52 and test probe card 53 results in the corresponding compliant response in respective first and second side laterally unsupported portions 248, 250 with electrical continuity between compliant portions 248, 250 being established by electrically conductive traces 272, 274 in combination with linking conductor 180.

Please replace paragraph number [0045] with the following rewritten paragraph:

[0045] FIG. 8 schematically illustrates a testing system 58 utilizing a contactor card-~~42~~ 342 which includes one or more compliant contacts according to the invention and as described above. A wafer-under-test-~~44~~ 344 having one or more contact pads thereon is operably coupled with the compliant contacts of contactor card-~~42~~ 342. The compliant contacts are also operably coupled with contact pads or other elements of a test probe card-~~50~~ 350 which is further operably coupled with a tester-~~52~~ 352 to form a ~~test~~ testing system 58. Contactor card-~~42~~ 342 may be physically coupled with wafer-under-test-~~44~~ 344 and/or the probe card-~~50~~ 350 through the use of a physical coupling mechanism known by those of ordinary skill in the art, and so not further described herein.

Please replace paragraph number [0046] with the following rewritten paragraph:

[0046] The foregoing description of specific embodiments of the present invention ~~have~~ has been presented for purposes of illustration and description. They are not intended to be exhaustive or to limit the invention to the precise forms disclosed, and many modifications and variations are possible in light of the above teaching. The embodiments were chosen and described in order to best explain the principles of the invention and its practical application, to thereby enable others of ordinary skill in the art to best utilize the invention and various

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embodiments with various modifications. It is intended that the scope of the invention be identified by the claims appended hereto and their equivalents.